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V_{DS} Ramp and HTRB Reliability Testing of High Power Semiconductor Devices with Automated Characterization Suite (ACS) Software

Introduction

Wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) offer physical properties superior to those of silicon (Si) for power device applications, enabling devices based on these materials to withstand high voltages and temperatures, as well as permitting higher frequency response, greater current density, and faster switching [1]. These emerging power devices have great potential; however, the technologies necessary to create and refine them are still under development and therefore less mature than silicon technology. This creates some big challenges associated with designing and characterizing these devices, as well as process monitoring and reliability issues [2].

Before they can gain commercial acceptance, the reliability of wide bandgap devices must be proven and there is a demand for higher reliability requirements. The continuous drive for greater power density at the device and package levels creates consequences in terms of higher temperatures and temperature gradients across the package. New application areas often mean more severe ambient conditions. For example, in automotive hybrid traction systems, the cooling liquid for the combustion engine may reach temperatures as high as 120°C. In order to provide sufficient margin, this means the maximum junction temperature (T_{JMAX}) must be increased from 150°C to 175°C [4]. In safety-critical applications such as aircraft, the zero-defect concept has been proposed to meet stricter reliability requirements.

V_{DS} Ramp and HTRB Reliability Tests

The V_{DS} ramp and the High Temperature Reverse Bias (HTRB) tests are among the most common reliability tests for power devices. In a V_{DS} ramp test, as the drain-source voltage is stepped from a low voltage to a voltage that's higher than the rated maximum drain-source voltage, specified device parameters are evaluated. The test is useful for tuning the design and process conditions, as well as verifying that devices deliver the performance specified on their data sheets. For example, Dynamic $R_{DS(ON)}$, monitored using a V_{DS} ramp test, provides a measurement of how much a device's ON-resistance increases after being subjected to a drain bias [5]. Although a V_{DS} ramp test is generally used as a quick form of parametric verification, an HTRB test evaluates long-term stability under high drain-source bias. During an HTRB test, the device samples are stressed at or slightly less than the maximum rated reverse breakdown voltage (usually 100% or 80% of V_{RRM}) at an ambient temperature close to their maximum rated junction temperature (T_{JMAX}) over a

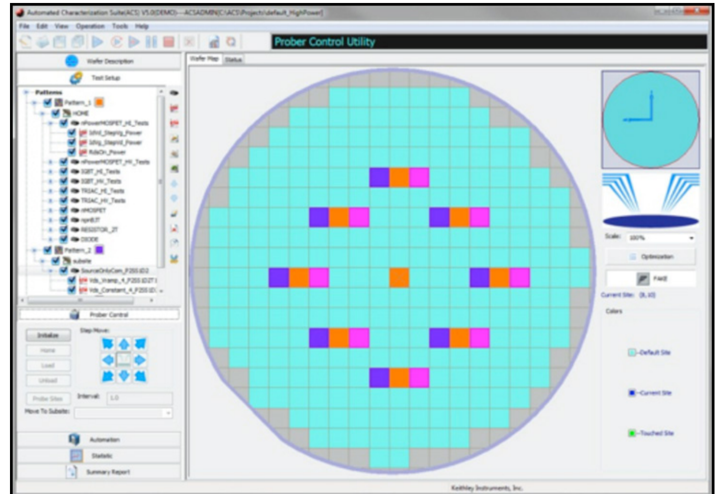

Figure 1. Automated Characterization Suite (ACS) graphical user interface

period of time (usually 1,000 hours)[3][5][6][7]. The leakage current is continuously monitored throughout the test and a fairly constant leakage current is generally required to pass the test. Because it combines electrical and thermal stress, this test can be used to check the junction integrity, crystal defects and ionic-contamination level, which can reveal weaknesses or degradation effects in the field depletion structures at the device edges and in the passivation [8].

Test Instrumentation and Measurement Considerations

Power device characterization and reliability testing require test instrumentation with higher voltage as well as more sensitive current measurement capability than ever before [2]. During operation, the devices undergo both electrical and thermal stress: when in the ON state, they have to pass tens or hundreds of amps with minimal loss (low voltage, high current); when they are OFF, they have to block thousands of volts with minimal leakage currents (high voltage, low current). Additionally, during the switching transient, they are subjected to a brief period of both high voltage and high current. The high current experienced during the ON state generates a large amount of heat, which may degrade device reliability if it is not dissipated efficiently [1].

Reliability tests typically involve high voltages, long test times, and often multiple devices under test (wafer level testing). As a result, well-designed test systems and measurement plans are essential to avoid breaking devices, damaging equipment, and losing test data. Consider the following factors when executing V_{DS} ramp and HTRB reliability tests:

- *Device connections:* When testing vertical devices with a common drain, proper connections are required to prevent stress termination in case of a single device breakdown.
- *Current limit control:* Current limit should allow for adjustment at breakdown to avoid damage to the probe card and device.
- *Stress control:* The high voltage stress must be well controlled to avoid overstressing the device, which can lead to unexpected device breakdown.
- *Proper test abort design:* The test program must be designed in a way that allows the user to abort the test (that is, terminate the test early) without losing the data already acquired.
- *Data management:* Effective data collection is essential to accommodate the large datasets due to long time and multi-site testing

A comprehensive hardware and software solution is essential to address these test considerations effectively. Keithley's Automated Characterization Suite (ACS) software supports semiconductor characterization at the device, wafer, and cassette levels. It offers users maximum flexibility for performing applications, so they can switch easily between manual operation for lab use and fully automated operation for production settings, using the same test plan. Its integrated test plan and wafer description function allow setting up single or multiple test plans on one wafer and selectively executing them later, either manually or automatically. ACS is compatible with many of Keithley's most advanced Source Measure Unit (SMU) instruments, including the Model 2636B (capable of sourcing up to 200V and measuring with 0.1fA resolution) and the high power Model 2657A (capable of sourcing up to 3kV and measuring with 1fA resolution).

Depending on the needs of the test environment, ACS systems can be configured to create anything from a simple system with a few instruments on a benchtop to an integrated, fully automated rack of instruments on a production floor. In addition to controlling Keithley SourceMeter® SMUs, other instruments, and switching hardware, ACS can control most standard automatic probers, execute the tests and return the resulting data for parameter extraction and analysis, all through a graphical user interface ***(Figure 1)***. The V_{DS} breakdown reliability test module for V_{DS} ramp and HTRB testing described in this application note is included in ACS Version 5.0 [9].

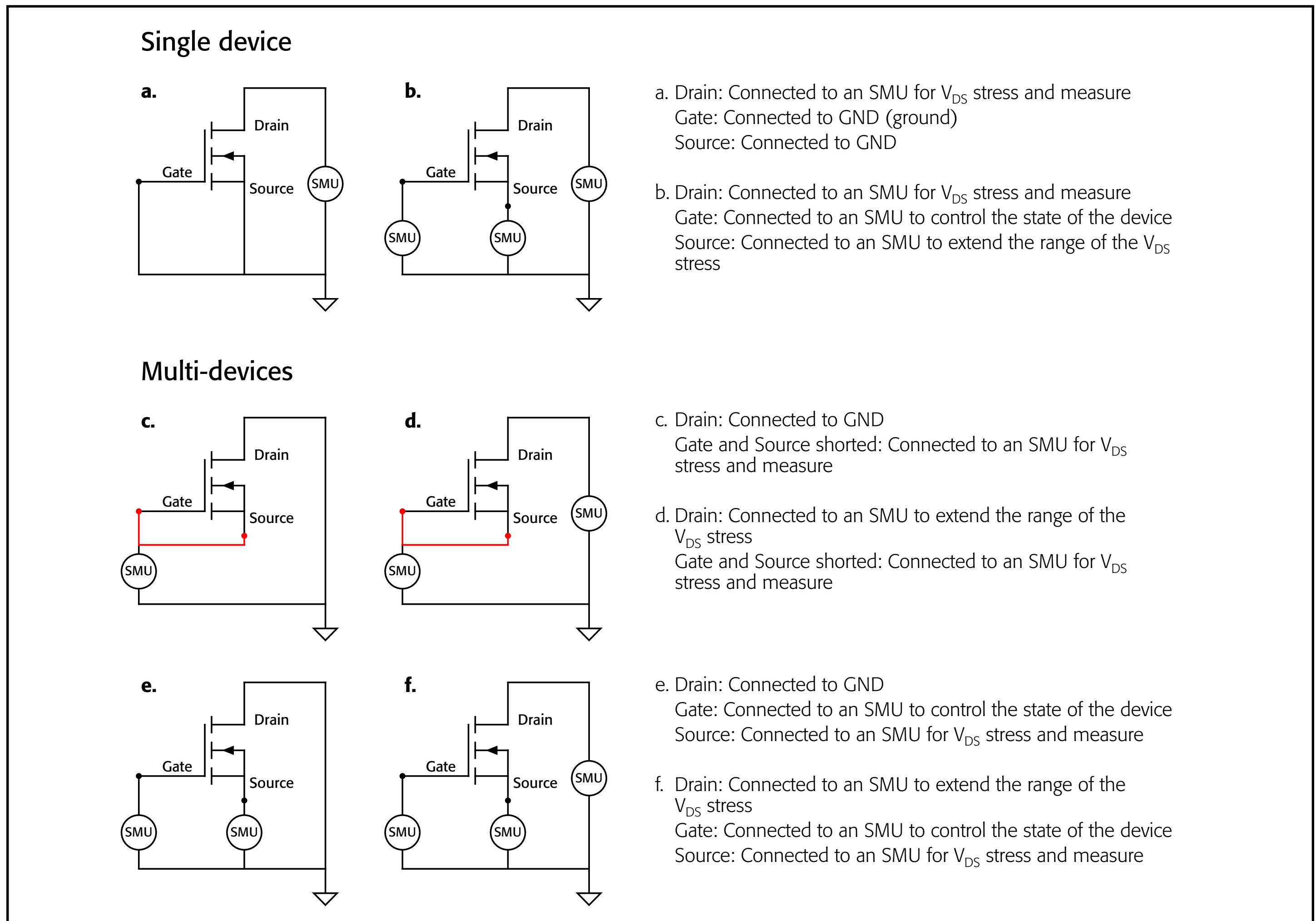

Figure 2. Various device connection options used with V_{DS} breakdown test module

ACS V_{DS} Breakdown Test Module

ACS's V_{DS} breakdown test module applies two different stress tests across the drain and source of the MOSFET structure (or across the collector and emitter of an IGBT) for V_{DS} ramp and HTRB reliability assessment:

Vds_Vramp – Applies ramped stress. This test sequence can be used as a quick method of parametric verification. The devices tested are evaluated on whether they meet the performance specifications listed on their data sheets.

Vds_Constant – Applies constant stress. This test sequence can be set up for reliability testing over an extended period and at elevated temperature, such as an HTRB test.

Device Connection

Depending on the number of instruments and devices, or the probe card type, users can implement various connection schemes ***(Figure 2)*** to achieve the desired stress configurations. When testing a single device, a user can apply voltage at the drain only for V_{DS} stress and measure, which requires only one SMU per device. Alternatively, a user can connect each gate and source to a SMU for more control in terms of measuring current at all terminals, extend the range of V_{DS} stress, and set voltage on the gate to simulate a practical circuit situation. For example, to evaluate the device in the OFF state (including HTRB test), V_{GS} might be set to $V_{GS} < 0$ for an N-channel depletion device, $V_{GS} > 0$ for a P-channel device, or $V_{GS} = 0$ for an enhancement-mode device.

For multi-device testing, careful consideration of device connections is essential. In a vertical device structure, the drain is common; therefore, it is not used for stress sourcing so that stress will not be terminated in case a single device breaks down. Instead, the source and gate are used to control stress.

Test Sequence

The *Vds_Vramp* test sequence has three stages: pre-test, main stress-measure, and post-test. Pre-test and post-test are optional. During the pre-test, a constant voltage is applied to verify the initial integrity of the body diode of the MOSFET; if the body diode is determined to be good, the test proceeds to the main stress-measure stage. Starting at a lower level, the drain-source voltage stress is applied to the device and ramps linearly to a point higher than the rated maximum voltage or until the user-specified breakdown criteria is reached. If the tested device is not broken at the main stress stage, the test proceeds to the next step, the post-test, in which a constant voltage is applied to evaluate the state of the device, similar to the pre-test. The measurements throughout the test sequence are made at both source and gate for multi-device testing (or drain for the single device case) and the breakdown criteria will be based on the current measured at source (or drain for a single device). The *Vds_Vramp* test sequence is useful for evaluating the effect of a drain-source bias on the device's parameters. ***Figure 3*** shows an example of a stress vs. time diagram for the main stress-measure stage of a *Vds_Vramp* test. (Pre-test and post-test are not shown.)

Although the *Vds_Vramp* sequence is generally used as a quick method of parametric verification, the *Vds_Constant* test sequence is suitable for long-term stability evaluations, such as HTRB, which normally run for an extended period at an elevated temperature. The *Vds_Constant* test sequence has a structure similar to that of the *Vds_Vramp* (that is, optional pre-test, main stress-measure, and optional post-test), with a constant voltage stress applied to the device during the stress stage and different breakdown settings. The stability of the leakage current I_{DSS} is monitored throughout the test. ***Figure 4*** shows an example stress vs. time diagram for the main stress-measure stage of a *Vds_Constant* test. (Pre-test and post-test are not shown.) Because this test requires evaluation over an extended period, the test module includes two features developed to prevent damage to the probe and device and to reduce the size of the dataset created: dynamic limit change and data compression.

Features to Solve Test Challenges

Several features of the ACS V_{DS} breakdown test module are designed to address the challenges commonly associated with V_{DS} ramp and HTRB reliability testing, namely the risk of device and equipment damage, device overstress and unexpected device breakdowns, the potential for data loss when aborting a test, and the management of large datasets. The following features offer solutions to these challenges: dynamic limit change, soft abort/bias, real-time post data, data compression, and graphic update suppression.

- **Dynamic limit change (current limit control)**
  A current limit can be set for the SMUs when applying the voltage. The output current will be clamped to the limit (compliance value) to prevent damage to the DUT. The high-level limit is usually set by estimating the maximum current during stress (for example, the current at the beginning of the stress). For most of the stress time, however, the current is much lower than the limit. When a breakdown occurs, there is no need to keep a high-level limit current running to that particular device because, over an extended time, the high-level current may melt the probe card tips and damage the devices. Dynamic limit change allows the current limit to vary according to the settings. The limit value can be set as a multiple of the measured current; in some cases, it can reduce the current by three orders of magnitude, which corresponds to 10^6 times lower in terms of power. This feature is implemented in the *Vds_Constant* test sequence (***Figure 6***).
- **Soft bias and soft abort (stress control and proper test abort design)**
  Soft bias/abort is an enhanced feature for protecting the measured device. This function allows the forced voltage or current to reach the desired value by ramping gradually at the start or the end of the stress, or when aborting the test, instead of changing suddenly. It helps to prevent in-rush currents and unexpected device breakdowns. In addition, it serves as a timing control over the process of applying stress.

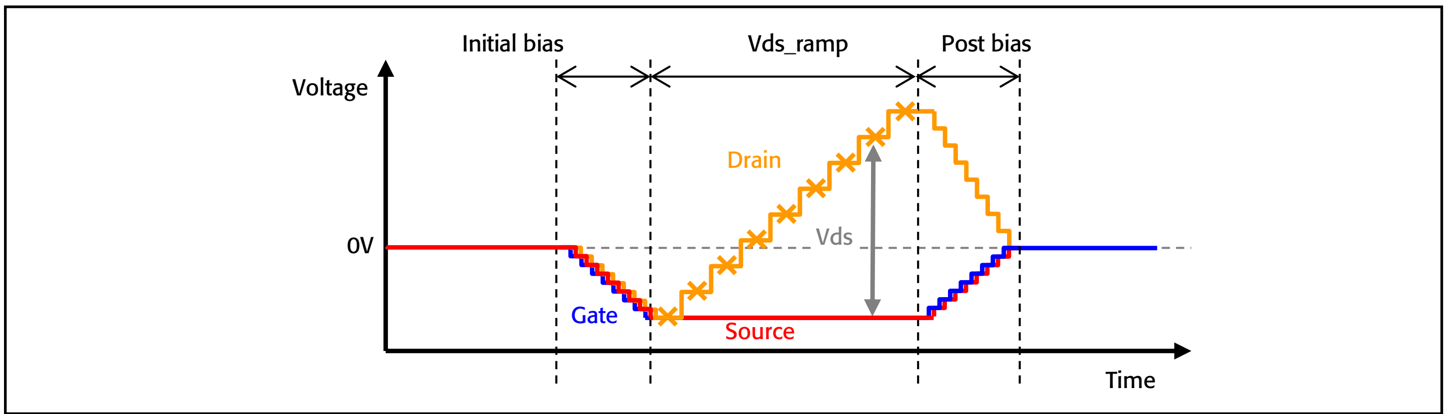

Figure 3. Stress vs. time diagram for *Vds_Vramp* test for a single device. Drain, gate and source are each connected to a Series 2600B SMU respectively. The drain is used for V_{DS} stress and measure; the V_{DS} range is extended by a positive bias on drain and a negative bias on source. A soft bias (gradual change of stress) is enabled at the beginning and end of the stress (initial bias and post bias). This test is used in conjunction with the device connection shown in *Figure 2b.* Measurements are performed at the "x" points.

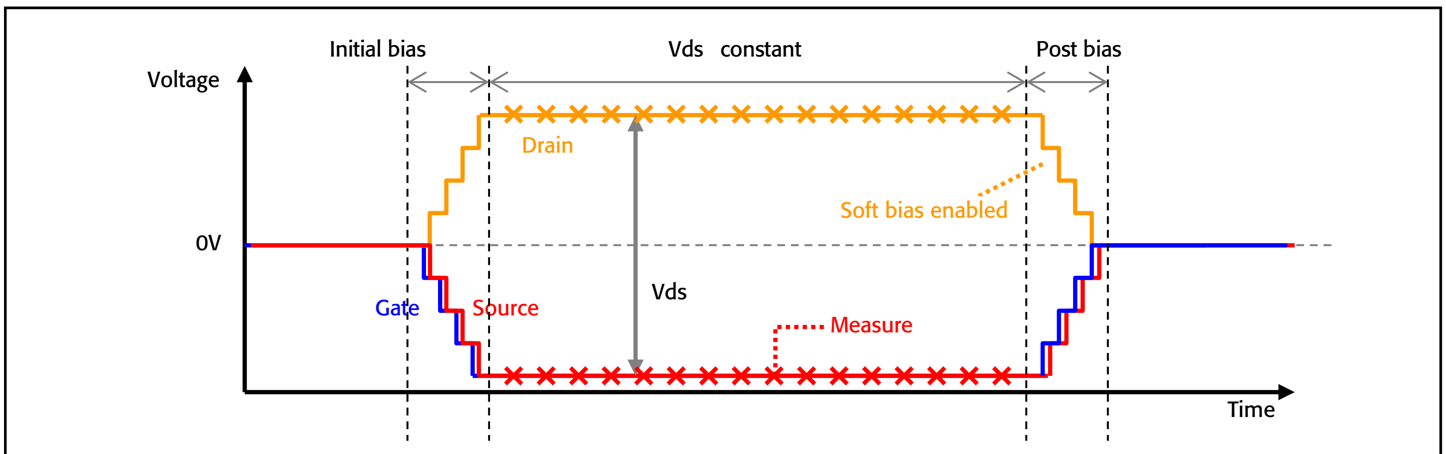

Figure 4. Stress vs. time diagram for *Vds_Constant* test sequence. The example is shown for vertical structure and multi-device case. Common drain, gate and source are each connected to a Series 2600B SMU respectively. The source is used for V_{DS} stress and measure; the V_{DS} range is extended by a positive bias on the drain and a negative bias on the source. A soft bias (gradual change of stress) is enabled at the beginning and end of the stress (initial bias and post bias). This test is used in conjunction with the device connection shown in *Figure 2f.* Measurements are performed at the "x" points.

As seen in *Figures 3 and 4*, the soft bias is enabled at the beginning and end of the stress.

The soft abort function works with a digital I/O module installed and connected to the test instrument. The digital I/O bit is set to LO after the user presses the abort button, and the LO bit input is sent to the software to invoke the soft abort function. The data will not be lost due to the data formatting at the termination of the test program. This is especially useful when the user does not want to continue the test as planned. For instance, imagine that 20 devices are being evaluated in a breakdown test for 10 hours and one of the tested devices exhibits abnormal behavior (such as substantial leakage current). The user will want to stop the test and redesign the test plan without losing the data that was taken for 10 hours. This feature is implemented in both the *Vds_Vramp* and *Vds_Constant* test modules ***(Figures 5* and *6).***

- **Real-time post data (data management and stress control**
This feature enables the user to select the test data to be posted and sent from the instruments to the ACS software after a specified time interval or when the desired number of points have been accumulated. When the *Vds_Vramp* sequence is used in a large-scale ramp test, which may use up to eight SMUs or other instruments, these settings ensure safe data logging and transfer. This is because data transfer via GPIB takes longer in multi-site testing than in single device testing. In addition, the master instrument controls data transactions between all other instruments and the host PC, as well as controlling the ramping rate of the stress. The time needed for communication might prevent ramping at the user-specified ramping rate.

Initially, test data is stored in instrument memory during testing, then transferred after the test is completed, which helps ensure the system uses the desired ramp rate. However, in some instances, the user will want to see the data graphed in real time, in order to check for irregularities and avoid human error or accidents.

The "real-time post data" option allows for manual control of data transfer. This balanced solution gives the user the

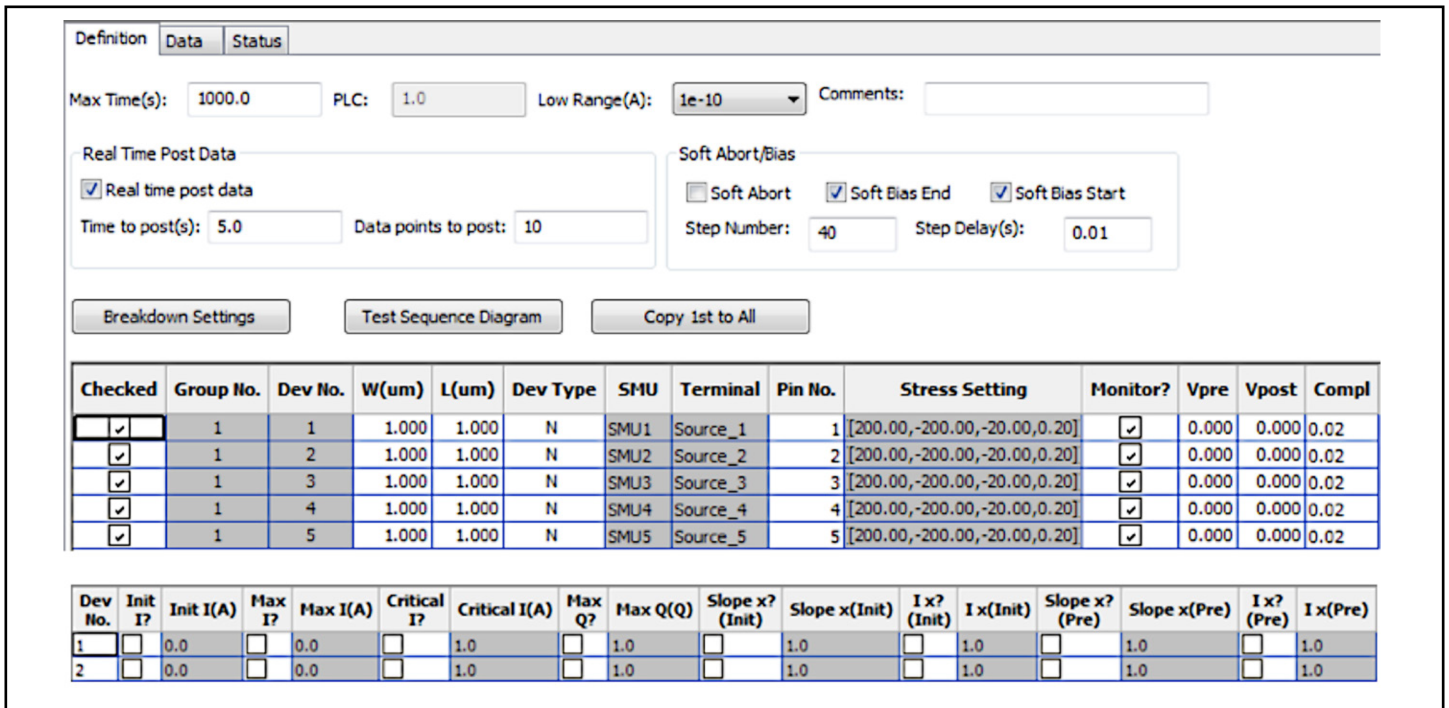

Figure 5. ***Vds_Vramp*** **test sequence**

Definition | Data | Status

Max Time(s): 10.0 PLC: 1.0

Low Range(A): 1e-10

Monitor

Sample Interval(s): 0.5

Hold Time(s): 0.0

Dynamic Limit

Enable Lowest Limit(A): 1e-008

Trigger Rate(%): 10.0 Limit Percent(%): 100.0

Current Limits

Jmax: 0.99 A/(um*um) J/J0: 1.0

qmax: 1.0 Q/(um*um) J/Jpre: 1.0

Soft Breakdown Limit: 1.0

Pre/Post Test

Pre/Post Test Meas Delay(s): 0.0

Jmax: 0.99 A/(um*um) Jmin: 0.1

Soft Abort/Bias

Soft Abort Soft Bias End Soft Bias Start

Step Number: 40 Step Delay(s): 0.01

Data Compression

Current Shift Shift Rate(%): 1.0 Time Log Points/Decade: 3

Lowest Line Lowest Line(A): 1e-008 Start(s): 100.0 Linear Constant Time(s): 10

Test Sequence Diagram | Copy 1st to All

Checked	Dev No.	W(um)	L(um)	SMU	Terminal	Pin No.	Compliance	Stress V	Monitor?	Pre/Post V
✓	1	1.00	1.00	SMU1	Source_1	1	0.01	-200	✓	0
✓	2	1.00	1.00	SMU2	Source_2	2	0.01	-200	✓	0
✓	3	1.00	1.00	SMU3	Source_3	3	0.01	-200	✓	0
✓	4	1.00	1.00	SMU4	Source_4	4	0.01	-200	✓	0
✓	5	1.00	1.00	SMU5	Source_5	5	0.01	-200	✓	0

Figure 6. ***Vds_Constant*** **test sequence**

advantage of both a real-time data check and ramp rate control. This feature is implemented in the *Vds_Vramp* test sequence ***(Figure 5)***.

- **Data compression (data management)**
  Reliability tests can run over many hours, days, or weeks, and have the potential to amass enormous datasets. Instead of collecting all the data produced, this function allows users to log only the data important to their particular work. Users can choose when to start data compression and how the data will be recorded by using the measured value or time settings. Data points can be logged when the current shift exceeds a specified percentage as compared to previously logged data and when the current is higher than a specified noise level. If the "time" setting is selected, the mean value of the data over the specified period or each value of the specified number of points per decade will be logged. This feature is implemented in the *Vds_Constant* test sequence ***(Figure 6).***
- **Suppress redundant graphic update (data management)**
  This practical function reduces the risks of working with large datasets by allowing users to specify that results graphics should NOT be refreshed automatically. This offers an effective way to avoid continuously and redundantly plotting and replotting a huge amount of data. The graph is updated only when the user requests it by pressing the "Refresh" button.

Conclusion

The V_{DS} ramp and HTRB tests are important power device reliability tools for parametric verification and long-term stability evaluation. The V_{DS} breakdown test module in ACS Version 5.0 includes two stress test sequences for V_{DS} ramp and HTRB reliability evaluation, which are enhanced with features that address common test challenges. The software and instrumentation in an ACS system are configurable for use in a wide variety of applications at the device, wafer, or cassette level, and in settings from a simple benchtop test setup to an automated, integrated rack of instruments. An optional ACS-2600-RTM package from Keithley offers additional reliability tests, including Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), voltage ramp (V_{Ramp}) test, and ramped current (J_{Ramp}) tests. Refer to the ACS-2600-RTM User's Manual for more information on these tests [10].

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