

Programmable Error Detector

PED3200 and PED4000 Series Datasheet



The PED3200 and PED4000 series programmable error detectors offer effective multi-channel BER for stressed receiver testing of data communications designs.

Key performance specifications

- Data rate range:
 - PED3200 series: 3 Gb/s to 32 Gb/s
 - PED4000 series: 4 Gb/s to 40 Gb/s

Key features

- Available with 1 or 2 input channels (independent data on each channel)
- PRBS and user defined patterns
- DC coupled differential data inputs (may also be used single ended or AC Coupled)

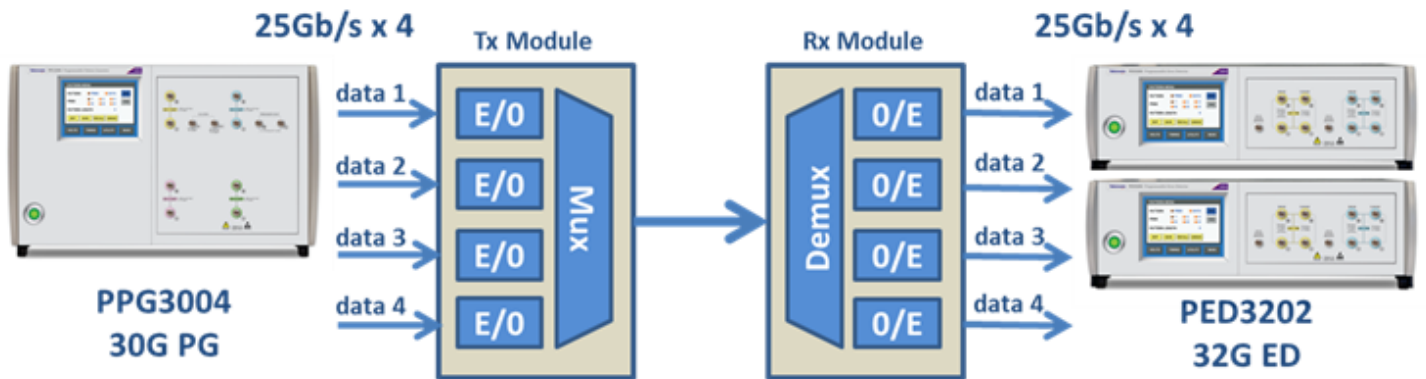
- Full rate AC coupled clock input (may also be used single ended)
- Auto-adjustment or manual adjustment of data to clock phase
- Auto-synchronization to input pattern
- Front panel touch screen GUI or USB TMC computer control

Applications

- 25 Gb/s testing for 100G Ethernet
- 32 Gb/s DPQPSK testing
- Semiconductor and component testing
- Design validation and production testing
- Transmitter testing and validation up to 40 Gb/s

Product description

The Tektronix PED line of high-performance error detectors offer single and two-channel standalone configurations capable of BER measurement at data rates up to 40 Gb/s. The PED products support either PRBS or user-defined data patterns, with simple to use automatic or manual alignment of input clock and data, and pattern synchronization. The PED product makes an ideal companion for the Tektronix PPG pattern generator product family.



100G Ethernet four lane end-to-end test using PED3200 series error detector and PPG3000 series pattern generator

Specifications

All specifications apply to all models unless noted otherwise.

Data input

Data rate

Range (PED3200)	3 Gb/s to 32 Gb/s
Range (PED4000)	4 Gb/s to 40 Gb/s

Amplitude

	DC-coupled CML input
Single-ended range	100 mV _{P-P} to 0.75 _{P-P}
Differential range	100 mV _{P-P} to 1.0 _{P-P}

Input voltage window range -0.6 V to +2.0 V for each input

Termination voltage 0 V

Clock input

Amplitude

	AC coupled, full rate
Differential range	300 mV _{P-P} to 1.0 V _{P-P}
Single-ended range	300 mV _{P-P} to 1.0 V _{P-P}

Clock to data phase adjustment 100 ps (-50 ps to +50 ps)

Data patterns

Pattern type

Data (from memory) or PRBS.
Length and type are individually settable on each channel.

Built-in PBRs patterns 2^n-1 (n = 7, 9, 11, 15, 23, 31)

User-defined pattern depth

Number of channels	Single bit pattern resolution
1 channel	4 Mbit
2 channels	2 Mbit

Mechanical

Front panel width (with mounting tabs) 48.3 cm (19.0 in)

Height 13.3 cm (5.25 in)

Width 45.1 cm (17.75 in)

Depth (rack mount) 34.3 cm (13.5 in)

Weight (1 channel) 11.1 kg (24.5 lbs)

Operating temperature 0 °C to 50 °C (32 °F to 122 °F)

Ordering information

Models

PED3201	32 Gb/s Programmable error detector, 1 channel
PED3202	32 Gb/s Programmable error detector, 2 channels
PED4001	40 Gb/s Programmable error detector, 1 channel
PED4002	40 Gb/s Programmable error detector, 2 channels

Options

Power plug options

Opt. A0	North America power plug (115 V, 60 Hz)
Opt. A1	Universal Euro power plug (220 V, 50 Hz)
Opt. A2	United Kingdom power plug (240 V, 50 Hz)
Opt. A6	Japan power plug (100 V, 110/120 V, 60 Hz)
Opt. A10	China power plug (50 Hz)
Opt. A11	India power plug (50 Hz)
Opt. A99	No power cord

User manual

Opt. L0	English manual
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Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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