Tektronix[®]

BSAPCI3 PCI 3.0 Receiver Test Software Datasheet



The BERTScope BSAPCI3 Automated PCIe 3.0 Receiver Solution is designed to streamline the tedious and labor-intensive receiver test workflow.

Features and benefits

- Automated calibration, link training, loopback initiation, and testing
- BER Map feature for TxEQ optimization
- Reduces the time and minimizes the skill-set required to perform the calibration and testing
- Increases the reliability and accuracy by removing inconsistencies with manual calibration

Applications

- PCIe 3.0 Receiver Testing for:
 - Host and device silicon validation
 - NVMe and SATA Express physical layer electrical testing
 - Add-in card and system compliance testing
 - Manufacturing test

Complete BERTScope automation for receiver testing

The BERTScope BSAPCI3 Automated PCIe 3.0 Receiver Solution is designed to streamline the tedious and labor-intensive receiver test workflow. No longer is expert PCIe 3.0 domain knowledge required to configure, calibrate, test, and document the results. Fast and accurate BERT-based testing provides high test throughput, intuitive and fast margin testing, and availability of a wide range of debugging tools when further testing is required. The result is high test productivity from setup through to the documentation of results.

This solution can also be used for the latest, emerging storage interfaces such as next-generation SSD and host controller interfaces that utilize NVMe and SATA Express protocols that reside on top of a PCIe 3.0 physical layer.

Test configuration wizard

The BERTScope BSAPCI3 Test Configuration Wizard provides step-bystep guidance for Receiver Test equipment setup and software setup. Clearly drawn block diagrams, cabling configurations, and descriptions simplify the test configuration setup.



Connection diagrams to help with test setups

BERTScope Address	169.254.31.99	Disconnect
Scope Address	169.254.46.27	Disconnect
test Server Address	169.254.46.27	Disconnect
Attempt connection to	Sigtest Server on 169.254.46.27:4006	
- Sigtest 3.1.70		
ownload Pattern Files	to BERTScope	
iles III Loooback	o barrocope	Duralized
JTOL Testin	a Gen	Download
SJ Calibratio	n	Check All
Eye-height	:al	Clear All
RJ Calibratio	n	Crear Ar
Reset JTOL	-	
Vinpitude C		

Connection wizard for instrumentation control and downloading of all required patterns

Automated stress calibration

An important step in preparing for receiver testing is the calibration of the stress sources to ensure that the stresss applied at the test fixture to the device under test is truly compliant with the test standard. In the past, these calibrations were often the most tedious and error-prone steps in the receiver test setup process. With the BSAPCI3 Automation Software, the calibration of the stress "recipe" is completely automated, including the calibration data. For test configurations that do not change, this step only needs to be performed once, and the stored calibration data is immediately available to be recalled. Engineers can spend less time calibrating, and more time testing.



Locating EH/EW targets





Calibration to final EH/EW targets



Automatic characterization and precise calibration of de-emphasis



Automatic characterization and precise calibration of preshoot



Automatic characterization and precise calibration of random jitter

Loopback initiation and link training

Before the receiver test can start, the device-under-test (DUT) must be put in the proper test mode, called Loopback, where the device is retransmitting the exact same data that was received. Entering Loopback mode is challenging because of the variety of loopback negotiation sequences across the range of PCIe 3.0 devices. The BERTScope BSAPCI3 Software provides various technique, including Link Training, to train and optimize the link for receiver testing.

Configure Loopback



Flexible link training and loopback control

BER map

One of the key challenges setting up the link is tuning or determining the optimal RxEQ settings. The BSAPCI3 BER Map feature provides an automated way to scan the PCIe 3.0 TxEQ coefficient matrix to determine the optimal TxEQ for a receiver's RxEQ settings.



Automated BER map result

Jitter tolerance testing

Jitter Tolerance testing is a critical part of the PCIe 3.0 receiver test and is a single-click operation with the BSAPCI3 Automation Software. With realtime stress adjustment, quick synchronization, and BER testing ability, the BERTScope provides the ideal platform for fast jitter compliance testing. Test results are stored using the built-in database for later recall and report generation.



PCIe 3.0 Jitter Tolerance test results

Beyond testing compliance, the automation software also provides a singleclick solution for finding the ultimate tolerance limits of the device under test, termed "search for margin".

Remote control protocol

The test software can be operated remotely through ASCII commands sent through TCP/IP, giving engineers further flexibility in designing "beyond compliance" tests.

Debugging tools

When a device fails to meet the test requirements, the operator has the power of the full range of BERTScope debugging tools. From intuitive and fast manual stress adjustment to the exclusive error analysis capability and jitter decomposition, the BERTScope can help identify subtle issues that other instruments might miss.

Test setup connection diagrams

The following diagrams show examples of some test setup connections. Icons/Item numbers in the diagrams refer to items described in the *Recommended* test fixtures, cables, and tools section towards the end of this datasheet.

CAUTION: When tightening cable connectors, to avoid damaging the connectors or cables, use only the SMA torque wrench (item 18) described in the *Recommended test fixtures, cables, and tools* section of this datasheet. When disconnecting the SMP cables from the test fixtures, use the SMP cable tool (item 19) described in the *Recommended test fixtures, cables, and tools* section of this datasheet.

Please refer to the following notes when indicated on the individual diagrams.

- Note 1: For PCIe Link Rx EQ capability, please connect the DPPLink cable (Tektronix part number, 174-6207-xx provided as a standard accessory to the DPP 125C) between the RS-232 connector on the rear panel of the DPP125C and the BSA-DPPLink connector on the rear of the BSA.
- Note 2: For system calibration, connect the SI Combiner output to CLB RX and oscilloscope to CBB TX (not shown).
- Note 3: For the PCIe Rx PLL Add-In-Card configuration, use 50 Ω SMA terminators on the Clock Recovery Module Data Output, standard accessory with the Clock Recovery Unit.
- Note 4: PCI-SIG recommends connecting a hard drive as a power load to your ATX power supply to ensure proper power delivery to your CBB3/CLB3 test fixtures.

DPP 125C Calibration Configuration



Item Description

- 9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- (11) SMA-to-SMA, Right Angle, 200 mm

Amplitude Calibration Configuration



- (9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- 10 SMA-to-SMA, Straight, 1000 mm, 1.5 ps phase-matched
- (11) SMA-to-SMA, Right Angle, 200 mm
- (14) SMA-to-SMA, 1.829 m

Add-In Card Eye Height/Width Calibration (See Note 2)



Item Description

- 1 CBB3 (Main)+(Riser)
- 2) x1/x16 CLB3
- 3 x4/x8 CLB3
- 4 Power supply
- (9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- (10) SMA-to-SMA, Straight, 1000 mm, 1.5 ps phase-matched
- (11) SMA-to-SMA, Right Angle, 200 mm
- (14) SMA-to-SMA, 1.829 m
- (15) SMA-to-SMP, Right Angle, 102 mm, 1 ps phase-matched

PCIe3-003

Add-In Card: Receiver Stressed Eye Testing



Item Description

- (1) CBB3 (Main)+(Riser)
- 4) Power supply
- (9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- 1) SMA-to-SMA, Right Angle, 200 mm
- (13) SMA-to-SMA, Right Angle, 500 mm
- (14) SMA-to-SMA, 1.829 m
- (15) SMA-to-SMP, Right Angle, 102 mm, 1 ps phase-matched
- (17) SMA-to-SMP, Right Angle, 1000 mm, 1 ps phase-matched

PCIe3-004

Note: Direction of the signal

Host (System): Receiver Stressed Eye Testing



Item Description

- 2) x1/x16 CLB3
- (3) x4/x8 CLB3
- (4) Power supply
- 9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- (11) SMA-to-SMA, Right Angle, 200 mm
- (12) SMA-to-SMA, Right Angle, 300 mm
- 13) SMA-to-SMA, Right Angle, 500 mm
- (14) SMA-to-SMA, 1.829 m
- (15) SMA-to-SMP, Right Angle, 102 mm, 1 ps phase-matched
- (17) SMA-to-SMP, Right Angle, 1000 mm, 1 ps phase-matched

PCIe3-005

PCIe Rx PLL Add-In Card



- 1) CBB3 (Main)+(Riser)
- 4) Power supply
- 9) SMA-to-SMA, Straight, 500 mm, 1.5 ps phase-matched
- (15) SMA-to-SMA, Right Angle, 102 mm, 1 ps phase-matched
- (16) SMA-to-SMP, Right Angle, 305 mm, 2.5 ps phase-matched
- (17) SMA-to-SMP, Right Angle, 1000 mm, 1 ps phase-matched

Ordering information

BSAPCI3 PCI 3.0 receiver test software	Automated calibration, link training, loop-back initiation, and test software for PCI 3.0 receiver test	
Product requirements	Tektronix BERTScope BSA85C or faster with Option STR	
	Tektronix DPP125C DPP with Option ECM	
	Tektronix CR125A or faster clock recovery with Option PCIE8G	
	Tektronix DPO/DSA/MSO71604C or faster Real-Time oscilloscope with Option DJA	
	For customers who need to perform Rx Link Eq testing, the RS-232 connector on the back of the BERTScope instrument must be labeled DPP LINK. BERTScope BSAxxxC instruments with serial numbers 280515 and above should already have DPP LINK installed. For BERTScope BSAxxxC instruments with serial numbers 280514 and below, the BSAxxxCUP COMUP upgrade must be installed by Tektronix Service to enable the DPP LINK high speed serial connection. Please contact your local Tektronix representative for more information.	
Host system software	Microsoft XP OS with SP2 or later	
requirements	Microsoft Explorer 6.0 SP1 or later	
	Microsoft Access	

Accessories

Recommended test fixtures, cables, and tools

The icon numbers in the following table refer to the items in the Test setup connection diagrams.





Datasheet





Datasheet





CE Marking Not Applicable.

(SRI) (SRI)

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Datasheet

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* European toll-free number. If not accessible, call: +41 52 675 3777

For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tektronix.com.

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